BK1080

Specifications

Beken Internal Data — Signed NDA Required for Distribution

FM Receiver IC

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1 General Description

The BK1080 FM receiver employs a low-IF architecture, mixed signal image rejection and all digital demodulation technology. The station scan of BK1080 searches radio stations based on both the channel RSSI estimation and signal quality assessment, increases the number of receivable stations while avoids false stops. BK1080 enables FM radio reception with low power, small board space and minimum number of external components.

All functions are controlled through a simple 3-wire serial interface or I2C serial interface. The device operates from a power supply of 2.7 – 5.5 volts.

The BK1080 is available in 24-pin 4x4 mm QFN, 20-pin 3x3 mm QFN, TSSOP16, SOP16 and SOP8 packages.

2 Features

- Support 65~108 MHz band
- Automatic gain control
- Automatic frequency control
- Seek tuning
- Receive signal strength indicator
- Channel quality assessment
- Stereo decoder
- Automatic stereo/mono switching
- Automatic noise suppression
- 50us/75us de-emphasis
- 2.5 ~ 5.5 V supply voltage
- Wide range reference clock supported
- 32.768KHz crystal oscillator
- I2C and 3-wires control interface
- 4x4 mm 24-pin QFN package
  3x3 mm 20-pin QFN package
  TSSOP 16-pin package
  SOP16-pin package
  SOP8-pin package

3 Applications

- Cellular handset
- MP3 player
- PDAs and notebook

4 Chip Block Diagram

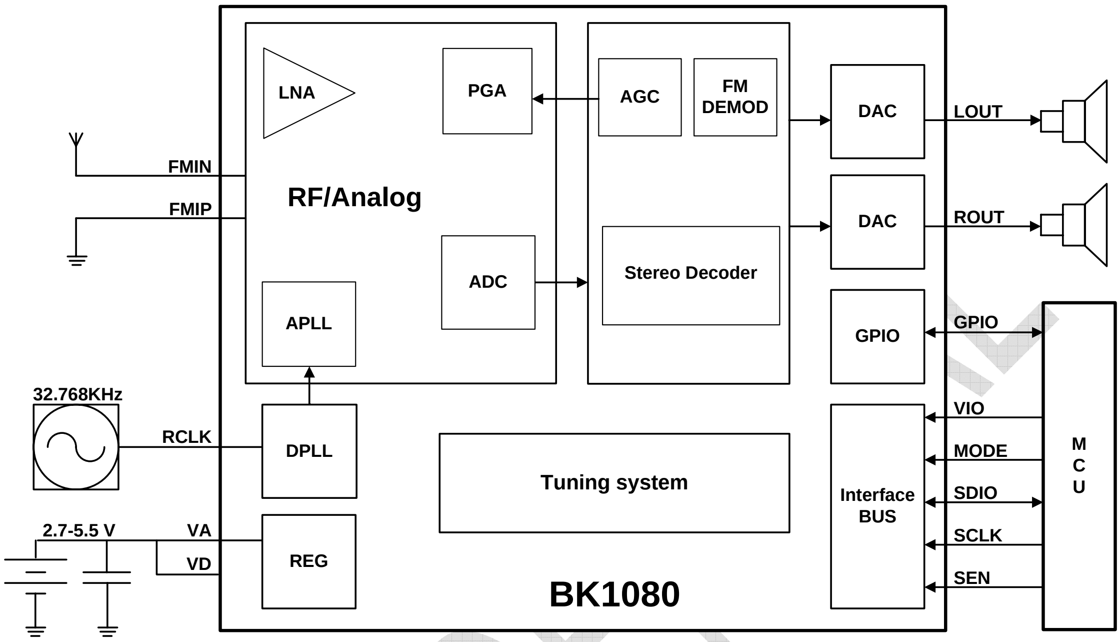


Figure 1 Chip Block Diagram

5 Pin Assignment

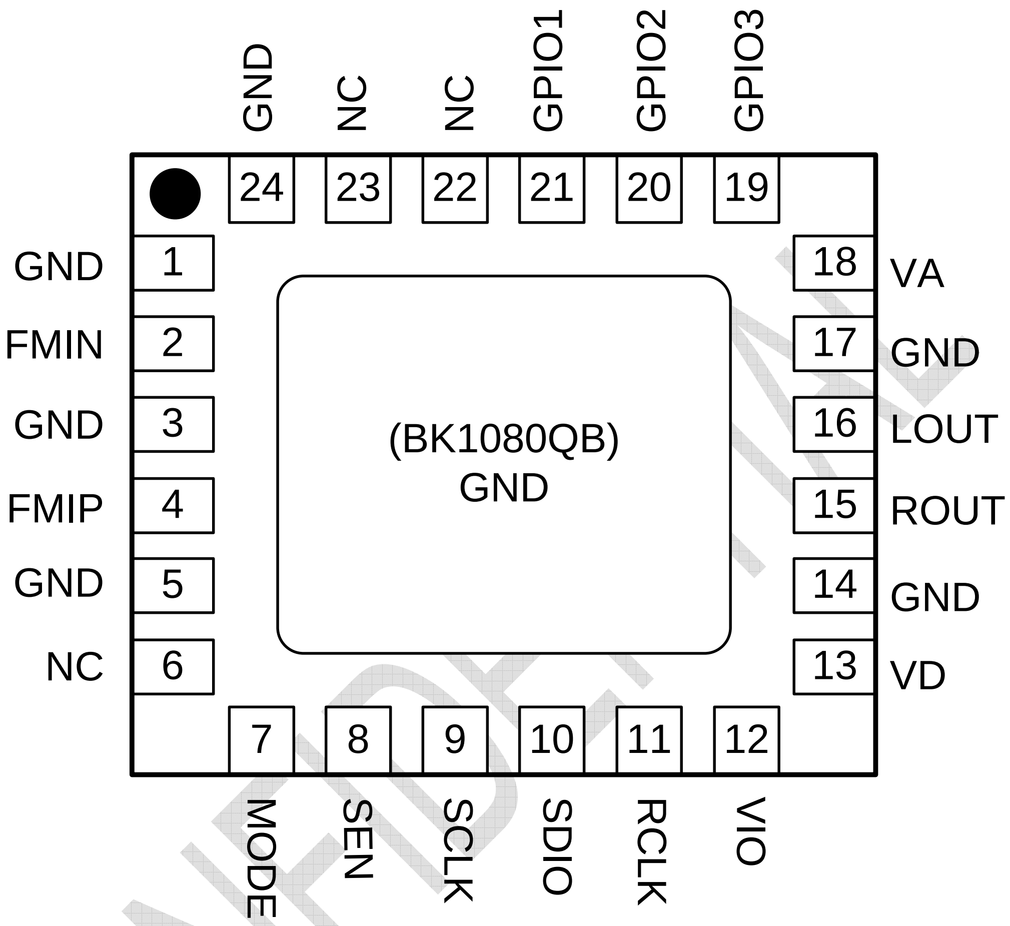


Figure 2 Pin Assignment for BK1080QB QFN24 4x4 mm package (top view)

Table 1 BK1080 QFN24 pin assignment

package Pin #	Name	Type	Description
1	GND	GND	RF ground.
2	FMIN[1]	RF	FM RF input negative port.
3	GND	GND	RF ground.
4	FMIP[1]	RF	FM RF input positive port.
5	GND	GND	I/O ground.
6	NC		Not connect.
7	MODE	I/O	Control Interface Select I2C interface is selected when the MODE pin is low 3-wire interface is selected when the MODE pin is high

8	SEN	I/O	Serial communications enable. (active low)
9	SCLK	I/O	Clock for Serial communications.
10	SDIO	I/O	Serial data input/output.
11	RCLK	I/O	External reference oscillator input.
12	VIO	P	Power supply for I/O.
13	VD	P	Power supply for digital.
14	GND	GND	Digital ground.
15	ROUT	AC	Right audio output.
16	LOUT	AC	Left audio output.
17	GND	GND	Analog ground.
18	VA	P	Power supply for analog.
19	GPIO3	I/O	General purpose output.
20	GPIO2	I/O	General purpose output.
21	GPIO1	I/O	General purpose output.
22	NC		Not connect.
23	NC		Not connect.
24	GND	GND	IF ground.

Note：

1. For single-ended input, one of FMIN and FMIP should be connected to ground

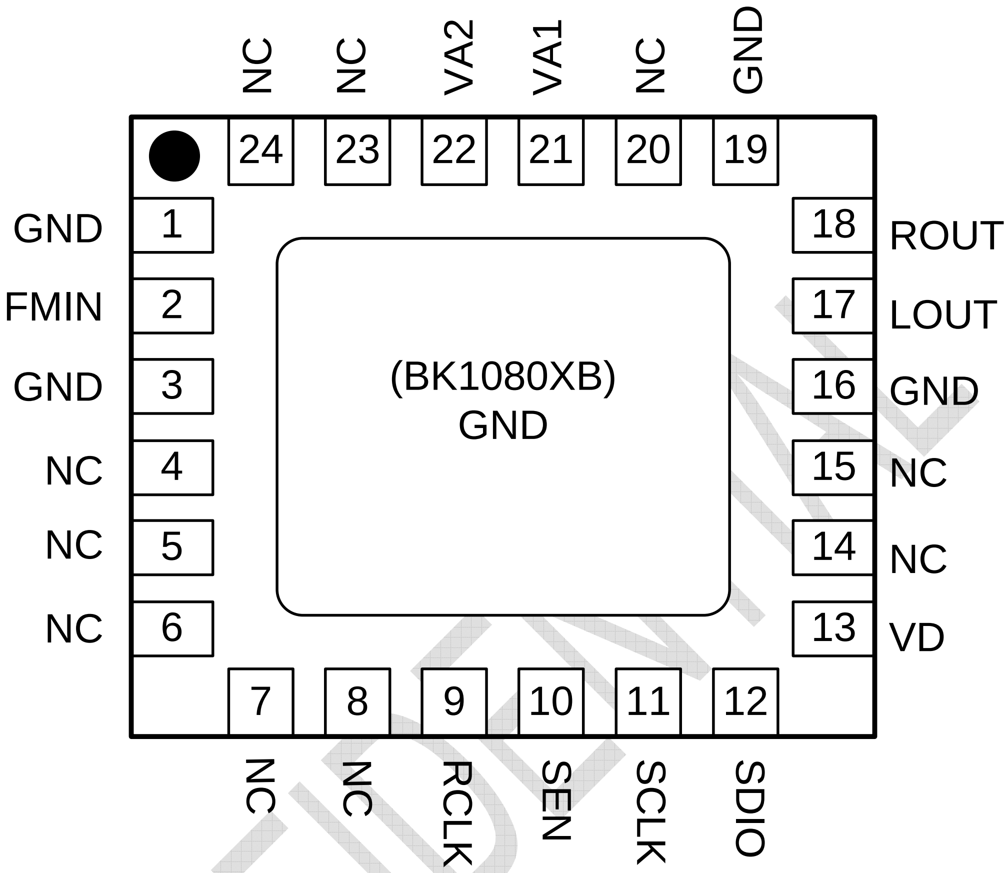


Figure 3 Pin Assignment for BK1080XB QFN24 4x4 mm package (top view)

Table 2 BK1080XB QFN24 pin assignment

package Pin #	Name	Type	Description
1	GND	GND	RF ground.
2	FMIN	RF	FM RF input negative port.
3	GND	GND	RF ground.
4	NC		Not connect.
5	NC		Not connect.
6	NC		Not connect.
7	NC		Not connect.
8	NC		Not connect.
9	RCLK	I/O	External reference clock or crystal oscillator input.
10	SEN	I/O	Serial communications enable. (active low)
11	SCLK	I/O	Clock for Serial communications.

12	SDIO	I/O	Serial data input/output.
13	VD	P	Power supply for digital and I/O.
14	NC		Not connect.
15	NC		Not connect.
16	GND	GND	Analog ground.
17	LOUT	AC	Left audio output.
18	ROUT	AC	Right audio output.
19	GND	GND	Analog ground.
20	NC		Not connect.
21	VA1	P	Power supply for analog.
22	VA2	P	Power supply for analog.
23	NC		Not connect.
24	NC		Not connect.

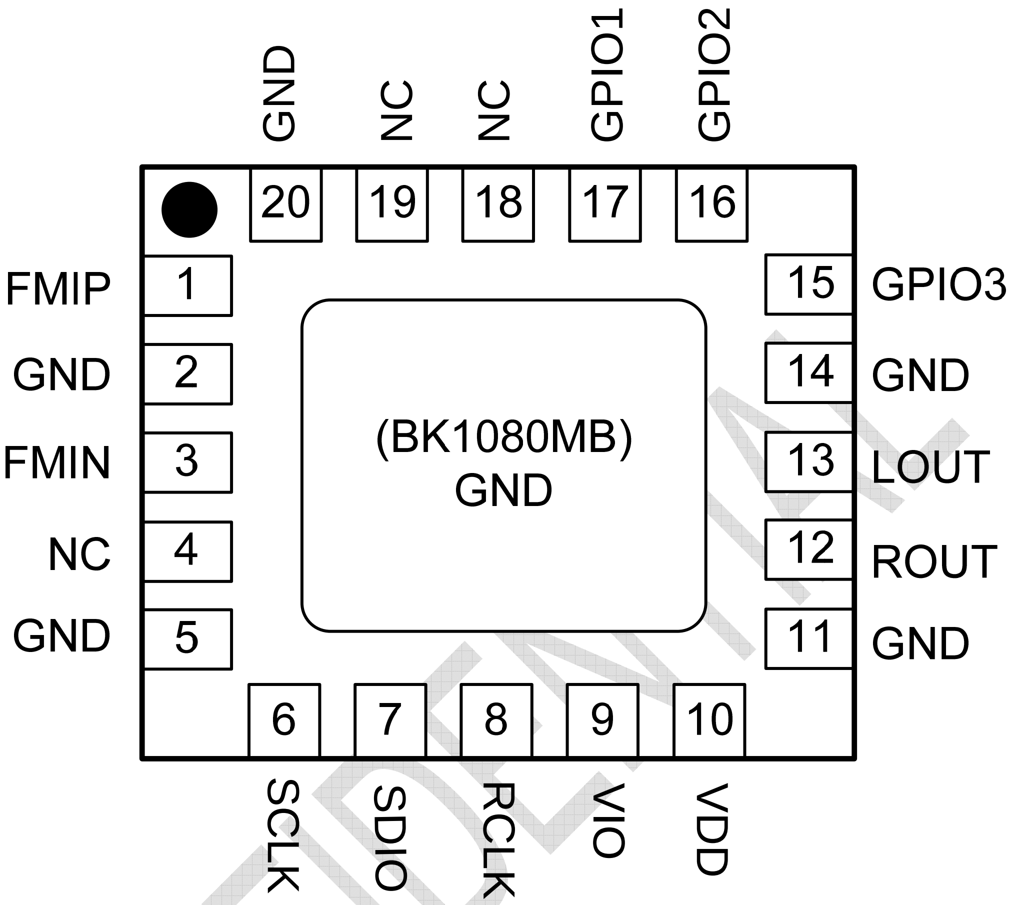


Figure 4 Pin Assignment for BK1080MB QFN20 3x3 mm package (top view)

Table 3 BK1080MB QFN20 pin assignment

package Pin #	Name	Type	Description
1	FMIP	RF	FM RF input positive port.
2	GND	GND	RF ground.
3	FMIN	RF	FM RF input negative port.
4	NC		Not connect.
5	GND	GND	I/O ground.
6	SCLK	I/O	Clock for Serial communications.
7	SDIO	I/O	Serial data input/output.
8	RCLK	I/O	External reference clock or crystal oscillator input.
9	VIO	P	Power supply for I/O.
10	VDD	P	Power supply for digital and analog.
11	GND	GND	Digital ground.

12	ROUT	AC	Serial data input/output.
13	LOUT	AC	Power supply for digital and I/O.
14	GND	GND	Analog ground.
15	GPIO3	I/O	General purpose output.
16	GPIO2	I/O	General purpose output.
17	GPIO1	I/O	General purpose output.
18	NC		Not connect.
19	NC		Not connect.
20	GND	GND	IF ground.

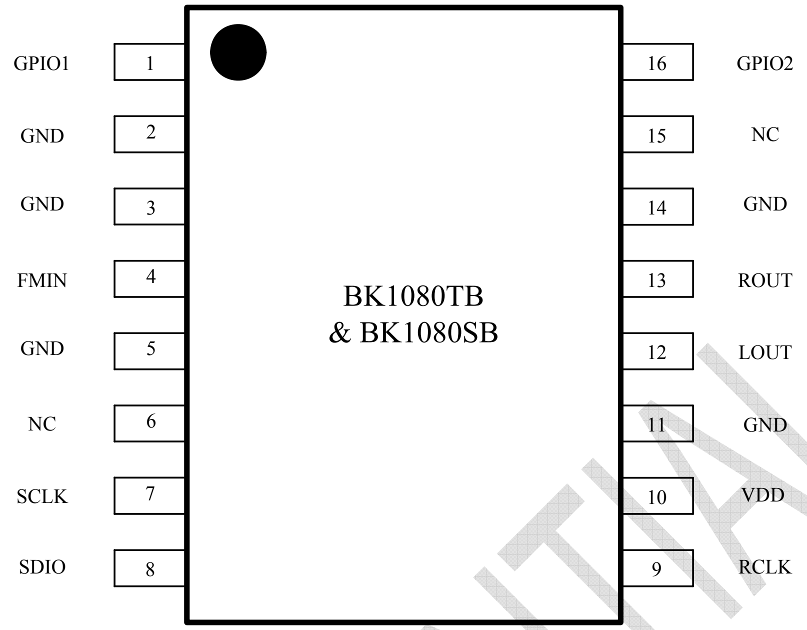


Figure 5 Pin Assignment for BK1080TB and BK1080SB package (top view)

Table 4 BK1080TB and BK1080SB pin assignment

package Pin #	Name	Type	Description
1	GPIO1	I/O	General purpose output.
2	GND	GND	RF ground.
3	GND	GND	RF ground.
4	FMIN	RF	FM RF input negative port.
5	GND	GND	RF ground.
6	NC	I/O	No connection
7	SCLK	I/O	Clock for Serial communications.
8	SDIO	I/O	Serial data input/output.
9	RCLK	I/O	External reference clock or crystal oscillator.
10	VDD	P	Power supply for digital and I/O.
11	GND	GND	Digital ground.
12	LOUT	AC	Left audio output.
13	ROUT	AC	Right audio output.
14	GND	GND	Analog ground.
15	VA	P	Power supply for analog.
16	GPIO2	I/O	General purpose output.

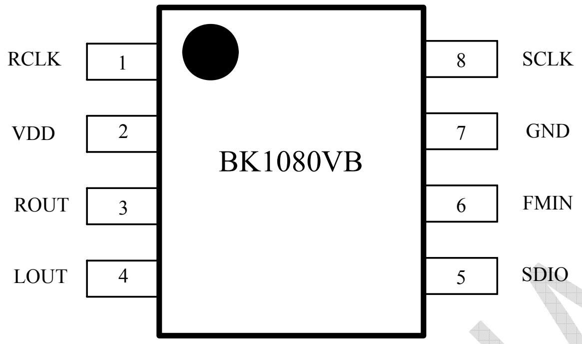


Figure 6 Pin Assignment for BK1080VB package (top view)

Table 5 BK1080VB pin assignment

package Pin #	Name	Type	Description
1	RCLK	I/O	External reference clock or crystal oscillator.
2	VDD	P	Power supply for digital and I/O.
3	ROUT	AC	Right audio output.
4	LOUT	AC	Left audio output.
5	SDIO	I/O	Serial data input/output.
6	FMIN	RF	FM RF input negative port.
7	GND	GND	RF ground.
8	SCLK	I/O	Clock for Serial communications.

6 Functional Description

6.1 FM Receiver

The receiver employs a digital low-IF architecture that reduces external components, and integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (65 to 108MHz), an automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers, an image-reject mixer down converts the RF signal to low-IF, The mixer output is amplified by a programmable gain control (PGA), and digitized by a high resolution analog-to-digital converters (ADCs). An audio DSP finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

6.2 Interface bus

The BK1080 supports 3-wire and I^2C control interface, with up to 2.5 MHz clock speed. User could select either of them by setting the state of MODE pin. BK1080 will use I2C interface for MODE=0 or 3-wire interface for MODE =1. Note that BK1080XB, BK1080MB, BK1080TB BK1080SB,and BK1080VB package only support I2C interface mode.

BK1080 always latches data at the rising edge of SCLK and outputs its data at the falling edge of SCLK. For MCU, data should be always written at the falling edge of SCLK, and read out at the rising edge of SCLK.

6.2.1 3-wire bus mode

When selecting 3-wire mode, user must set MODE = 1.

3-wire bus mode uses SCLK, SDIO and SEN pins. A transaction begins when user drives SEN low. Next, user drives an 8-bit command serially on SDIO, which is captured by BK1080 on rising edges of SCLK. The command consists of a 7-bit start register address, followed by a read/write bit (read = 1, write = 0).

6.2.2 I2C bus mode

When selecting I2C mode, user must set MODE = 0.

I2C bus mode only uses SCLK and SDIO pins. A transaction begins with the start condition, which occurs when SDIO falls while SCLK is high. Next, user drivers an 8-bit device ID serially on SDIO, which is captured by BK1080 at the rising edge of SCLK. The device ID of BK1080 is 0x80.

After driving the device ID, user drives an 8-bit control word on SDIO. The control word consists of a 7-bit start register address, followed by a read/write bit (read = 1, write = 0).

For I2C host reading, the host must give an ACK to BK1080 after each byte access, and should give a NACK to BK1080 after last byte read out.

For stable communication, the rising edge time of SCLK should be less than 200ns.

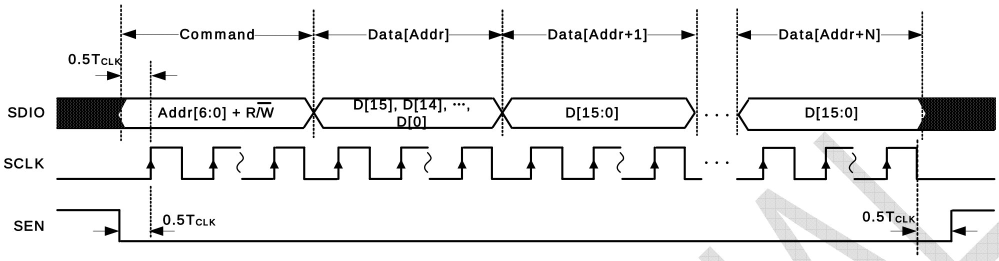


Figure 7 3-wire Interface Diagram

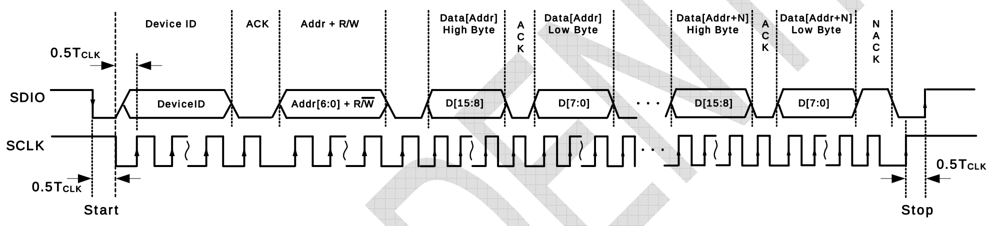


Figure 8 I2C Interface Diagram

6.3 Stereo audio processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. MPX signal format consists of left + right (L+R) audio, left –right (L–R) audio, a 19 kHz pilot tone.

The BK1080 has integrated stereo decoder automatically decodes the MPX signal. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L-R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L-R) signal. Separate left and right channels are obtained by adding and subtracting the (L+R) and (L-R) signals, respectively. Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. The signal level range over which the stereo to mono blending occurs can be adjusted by setting the BLNDADJ [1:0] register. Stereo/mono status can be monitored with the ST register bit and mono operation can be forced with the MONO register bit.

BK1080 uses pre-emphasis and de-emphasis to improve the signal-to-noise ratio of FM receivers by reducing the effects of high frequency interference and noise. When the FM signal is

transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants, 50 or 75 µs, are used in various regions. The de-emphasis time constant is programmable with the DE bit. High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted with the DMUTE bit. Volume can be adjusted digitally with the VOLUME [3:0] bits. The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The soft mute attack and decay rate can be adjusted with the SMUTER [1:0] bits where 00 is the fastest setting. The soft mute attenuation level can be adjusted with the SMUTEA [1:0] bits where 00 is the most attenuated. The soft mute disable (DSMUTE) bit may be set high to disable this feature.

6.4 Tuning System

Channel spacing of 50, 100 or 200 kHz is selected with bits SPACE [1:0]. The channel is selected with bits CHAN [9:0]. The bottom of the band is set to 76 MHz or 87.5 MHz with the bits BAND [1:0]. The tuning operation begins by setting the TUNE bit. After tuning completes, the seek/tune complete (STC) bit will be set and the RSSI level is available by reading bits RSSI [7:0]. The TUNE bit must be set low after the STC bit is set high in order to complete the tune operation and clear the STC bit. Seek tuning searches up or down for a channel with an RSSI greater than or equal to the seek threshold set with the SEEKTH [7:0] bits. In addition, an optional SNR and/or impulse noise detector may be used to qualify valid stations. The SKSNR [3:0] bits set the SNR threshold required. The SKCNT [3:0] bits set the impulse noise threshold. Using the extra seek qualifiers can reduce false stops and, in combination with lowering the RSSI seek threshold, increase the number of found stations. The SNR and impulse noise detectors are disabled by default. Two seek modes are available. When the seek mode (SKMODE) bit is low and a seek operation is initiated, the device seeks through the band, wraps from one band edge to the other, and continues seeking. If the seek operation was unable to find a channel, the seek failure/band limit (SF/BL) bit will be set high and the device will return to the channel selected before the seek operation began. When the SKMODE bit is high and a seek operation is initiated, the device seeks through the band until the band limit is reached and the SF/BL bit will be set high. A seek operation is initiated by setting the SEEK and SEEKUP bits. After the seek operation completes, the STC bit will be set, and the RSSI level and tuned channel are available by reading bits RSSI [7:0] and bits READCHAN [9:0]. During a seek operation READCHAN [9:0] is also updated and may be read to determine seek progress. The STC bit will be set after the seek operation completes. The channel is valid if the seek operation completes and the SF/BL bit is set low. At other times, such as before a seek operation or after a seek completes and the SF/BL bit is set high, the channel is valid if the AFC Rail (AFCRL) bit is set low and the value of RSSI [7:0] is greater than or equal to SEEKTH [7:0]. Note that if the AFCRL bit is set, the

audio output is muted as in the soft mute case discussed in stereo audio processing section. The SEEK bit must be set low after the STC bit is set high in order to complete the seek operation and clear the STC and SF/BL bits. The seek operation may be aborted by setting the SEEK bit low at any time. The device can be configured to generate an interrupt on GPIO2 when a tune or seek operation completes. Setting the seek/tune complete (STCIEN) bit and GPIO2 [1:0] = 01 will configure GPIO2 for a 5 ms low interrupt when the STC bit is set by the device.

6.5 Software Tuning System

The BK1080 also supports the software seek by tuning and judging every channels from MCU. The operation begins by setting the TUNE bit after tuning completes, the seek/tune complete (STC) bit will be set and the RSSI, SNR , IMPC and FREQD level is available by reading bits RSSI [7:0], SNR[3:0], IMPC[3:0] and FREQD[11:0].When all this parameters meet the thresholds which can set by MCU, it is a right station.

6.6 GPIO Output

The BK1080 has three GPIO pins. The function of GPIO pins could be programmed with bits GPIO1 [1:0], GPIO2 [1:0], GPIO3 [1:0], GPIO2/3 pins can be used as interrupt request pins for the seek/tune ready functions and as a stereo/mono indicator respectively.
General purpose output functionality is available regardless of the state of the VA and VD supplies, or the ENABLE and DISABLE bits.

6.7 Reference clock

The BK1080 series accepts wide range, from 32.768 kHz to 38.4 MHz, reference clock input to the RCLK pin. For frequency less than 4 MHz, it must be multiplier of 32.768K. The BK1080 series requires the $V_{pk\text{-}pk}$ of reference clock is higher than 500mV. BK1080 also support wide range crystal oscillator input.

6.8 Initialization Sequence

To initialize BK1080:
1. Supply VIO.
2. Supply VA and VD. Note that VA and VD could be supplied at the same time of VIO supplied.
3. Provide RCLK.
4. Set the ENABLE bit high and the DISABLE bit low to power up BK1080.

To power down BK1080:
1. Set the ENABLE bit high and the DISABLE bit high to place BK1080 in power down mode. Note that all register states are maintained so long as VIO is supplied.
2. (Optional) Remove RCLK.
3. Remove VA and VD as needed.

To power up BK1080 (after power down):
1. Note that VIO is still supplied in this scenario. If VIO is not supplied, refer to BK1080 initialization procedure above.
2. Supply VA and VD.
3. Provide RCLK.

4. Set the ENABLE bit high and the DISABLE bit low to power up BK1080.

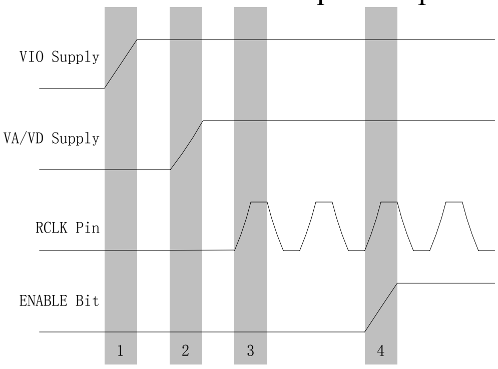


Figure 9 Initialization Sequence

7 Design Specification

7.1 Recommended Operating Conditions

Table 6 Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage	V_D		2.5	—	5.5	V
Analog Supply Voltage	V_A		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.6	—	3.6	V
Ambient Temperature	T_A		–20	25	85	°C
Notes: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_D = V_A = 3.3$ V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated. For BK1080XB, BK1080TB,BK1080SB and BK1080VB packages ,Supply Voltage range is 2.7V-3.6V						

7.2 Power Consumption Specification

Table 7 Power Consumption Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_S	ENABLE = 1 DISABLE = 0	—	20	22	mA
Power down Current	I_{PD}	ENABLE = 0 DISABLE = 1	—	10	20	µA
Interface Power down Current	Ip_{IO}	SCLK, RCLK inactive ENABLE = 0	—	1.9	5	µA

7.3 Receiver Characteristics

Table 8 Receiver Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Input Frequency [14]		64	—	108	MHz
Sensitivity[2, 3, 4,5]	(S+N)/N = 26 dB	—	1.5	2.5	µV EMF
LNA Input Resistance[7]		2.5	3	3.5	kΩ
Input IP3[8]		90	95	—	dBµV EMF
AM Suppression[2, 3, 4, 5, 7]	m = 0.3	40	45	—	dB
Adjacent Channel Selectivity	±200 kHz	40	50	—	dB
Alternate Channel Selectivity	±400 kHz	50	60	—	dB
Audio Output Voltage[2, 3, 4, 7]		—	100	—	mVRMS
Audio Stereo Separation[2, 4, 5, 7]		30	40	—	dB
Audio S/N[2, 3, 4, 5, 7, 13]			60	—	dB
Audio THD[2, 3, 5, 7, 10]		—	0.2	0.5	%
Audio Common Mode Voltage[12]	ENABLE = 1	1.1	1.2	1.3	V
Audio Output Load Resistance	Single-ended	—	32	—	Ω
Seek/Tune Time		—	—	60	ms/channel
RSSI Offset	Input levels of 8 and 50 dBµV at RF input	–3	—	3	dB

Notes:

1. Volume = maximum for all tests
2. F_{MOD} = 1 kHz, 75 µs de-emphasis
3. MONO = 1, and L = R unless noted otherwise
4. Δf = 22.5 kHz
5. B_{AF} = 300 Hz to 15 kHz, A-weighted
6. Sensitivity without matching network
7. Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz
8. |f2 – f1| > 1 MHz, f0 = 2 x f1 – f2. AGC is disabled by setting AGCD = 1
9. The channel spacing is selected with the SPACE [1:0] bits
10. Δf = 75 kHz
11. The de-emphasis time constant is selected with the DE bit
12. At LOUT and ROUT pins
13. Guaranteed by reference clock performance
14. For BK1080QB,frequency range is 76Mhz to 108MHz

7.4 I2C Control Interface Characteristics

Table 9 I2C Control Interface Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		—	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6			µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold	$t_{HD:DAT}$		—	—	900	ns
SCLK Input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		—	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		—	—	200	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	60	pF
Input Filter Pulse Suppression	t_{SP}		—	—	40	ns

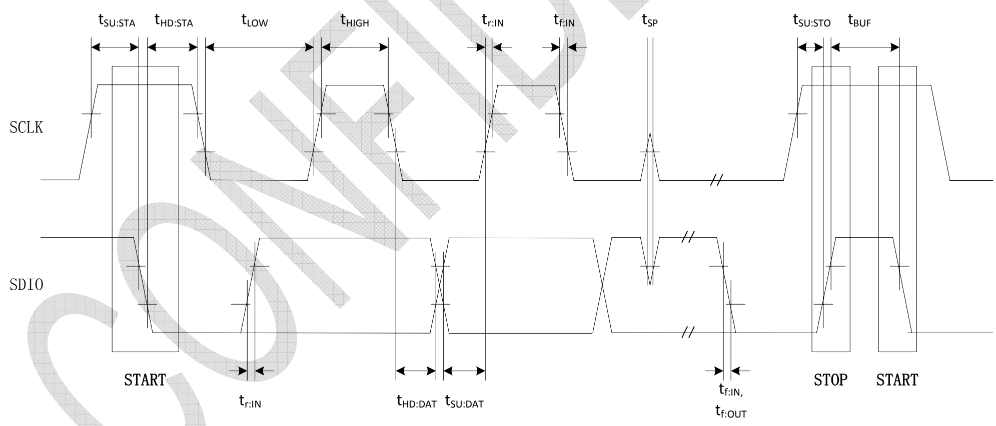


Figure 10 I2C Control Interface Read and Write Timing Diagram

7.5 3-Wire Control Interface Characteristics

Table 10 3-Wire Control Interface Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, SEN to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
SEN Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, SEN, SDIO, Rise/Fall Time	t_R , t_F		—	—	10	ns

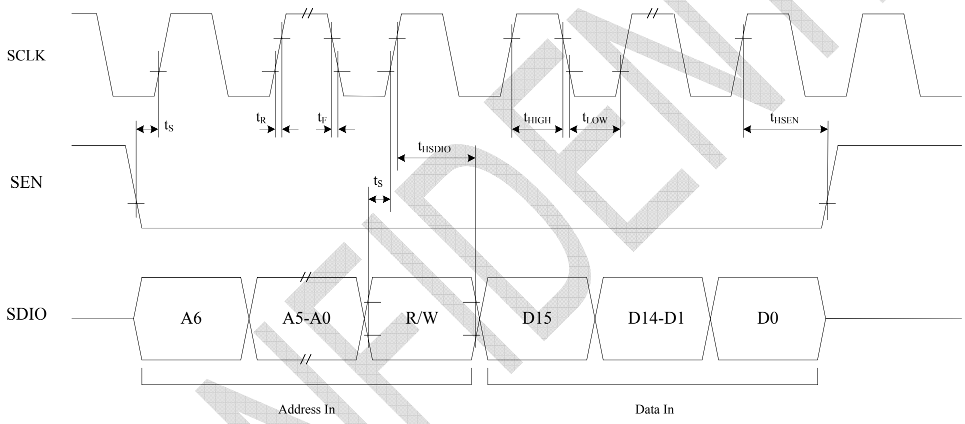


Figure 11 3-Wire Control Interface Write Timing Diagram

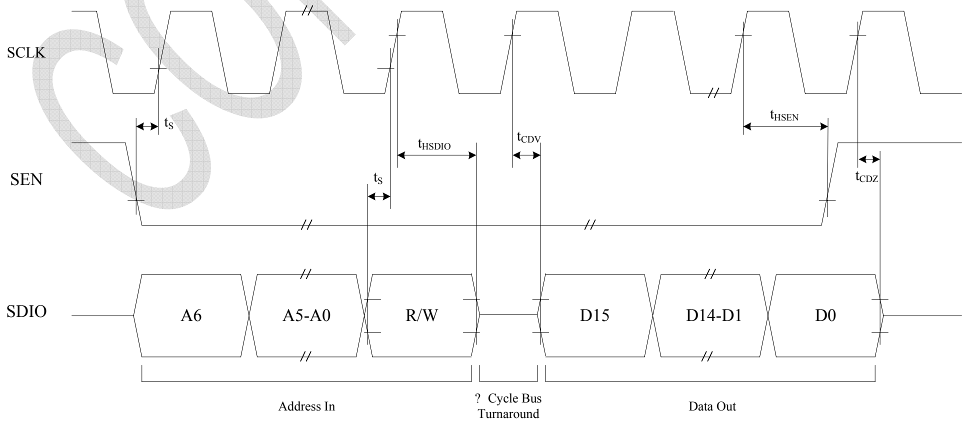


Figure 12 3-Wire Control Interface Read Timing Diagram

8 Register definition

Table 11 Register definition

Register Name	Address	Dir	Name	Bits	Default (Hex)	Description
REG0	00h	R	No Use, Default value: 0x0006			
				15:0	0x0006	Always 0
REG1	01h	R	No Use, Default value: 0x1080 for 2009 Jan. Release			
			Chip ID	15:0	0x1080	Different in different version
REG2	02h	R/W	Power configuration, Default value: 0x0000			
			DSMUTE	15	0	Soft mute Disable 0 = Soft mute enable (default) 1 = Soft mute disable
			MUTE	14	0	Mute 0 = Dismute (default) 1 = Mute
			MONO	13	0	Mono Select 0 = Stereo (default) 1 = Force mono
			CKSEL	12	0	Clock Select 0 = External clock 1 = Internal crystal oscillator
			Reserved	11	0	Reserved. Always write to 0
			SKMODE	10	0	Seek Mode 0 = Wrap at the upper or lower band limit and continue seeking (default) 1 = Stop seeking at the upper or lower band limit
			SEEKUP	9	0	Seek Direction. 0 = Seek down (default). 1 = Seek up.
			SEEK	8	0	Seek. 0 = Disable (default) 1 = Enable Notes: 1. Seek begins at the current channel, and goes in the direction specified with the SEEKUP bit. Seek operation stops when a channel is qualified as valid according to the seek parameters, the entire band has been searched (SKMODE = 0), or the upper or lower band limit has been reached (SKMODE = 1) 2. The STC bit is set high when the seek operation completes and/or the SF/BL bit is set high if the seek operation was unable to find a channel qualified as valid according to the seek parameters. The STC and SF/BL bits must be set low by setting the SEEK bit low before the next seek or tune may begin 3. Seek performance for 50 kHz channel spacing varies according to RCLK tolerance. Beken recommends ±50 ppm RCLK crystal tolerance for 50 kHz seek performance 4. A seek operation may be aborted by setting SEEK = 0
			Reserved	7	0	Reserved, always write to 0

Register Name	Address	Dir	Name	Bits	Default (Hex)	Description
			Disable	6	0	Power up disable
			Reserved	5:1	0	Reserved, always write to 0
			ENABLE	0	0	Power up Enable
REG3	**03h**	**R/W**	**Channel. Default value: 0x0000**			
			TUNE	15	0	Tune. 0 = Disable (default) 1 = Enable The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The STC bit must be set low by setting the TUNE bit low before the next tune or seek may begin
			Reserved	14:10	0	Reserved, always write to 0
			CHAN<9:0>	9:0	0	Channel Select Channel value for tune operation If BAND 05h[7:6] = 00, then Freq (MHz) = Spacing (kHz) x Channel + 87.5 MHz If BAND 05h[7:6] = 01, BAND 05h[7:6] = 10, then Freq (MHz) = Spacing (kHz) x Channel + 76 MHz CHAN[9:0] is not updated during a seek operation. READCHAN[9:0] provides the current tuned channel and is updated during a seek operation and after a seek or tune operation completes. Channel spacing is set with the bits SPACE 05h[5:4]
REG4	**04h**	**R/W**	**System configuration 1. Default value: 0x0000**			
			Reserved	15	0	Reserved, always write to 0
			STCIEN	14	0	Seek/Tune Complete Interrupt Enable 0 = Disable Interrupt (default) 1 = Enable Interrupt Setting STCIEN = 1 and GPIO2[1:0] = 01 will generate a 5 ms low pulse on GPIO2 when the STC 0Ah[14] bit is set
			DEBPS	13	0	Bypass De-emphasis filter 0: Enable 1: Bypass
			Reserved	12	0	Reserved, always write to 0
			DE	11	0	De-emphasis 0 = 75 µs. Used in USA (default) 1 = 50 µs. Used in Europe, Australia, Japan.
			AGCD	10	0	AGC Disable 0 = AGC enable (default) 1 = AGC disable
			Reserved	9:8	0	Reserved, always write to 0
			BLNDADJ<1:0>	7:6	0	Stereo/Mono Blend Level Adjustment Sets the RSSI range for stereo/mono blend 00 = 31–49 RSSI dBµV (default) 01 = 37–55 RSSI dBµV (+6 dB) 10 = 19–37 RSSI dBµV (–12 dB) 11 = 25–43 RSSI dBµV (–6 dB) ST bit set for RSSI values greater than low end of range

Register Name	Address	Dir	Name	Bits	Default (Hex)	Description
			GPIO3<1:0>	5:4	0	00 = Low (default) 01 = Stereo Decoder Indicator (STEN). The GPIO3 will output logic high when the device is in stereo demodulating status, otherwise the device will output a logic low for mono 10 = Low 11 = High
			GPIO2<1:0>	3:2	0	00 = Low (default) 01 = STC interrupt. Logic high will be output unless an interrupt occurs as described below 10 = Low 11 = High Setting STCIEN = 1 will generate a 5 ms low pulse on GPIO2 when the STC 0Ah[14] bit is set.
			GPIO1<1:0>	1:0	0	00 = Low (default) 01 = Reserved 10 = Low 11 = High
REG5	05h	R/W	System configuration 2. Default value: 0x0000			
			SEEKTH<7:0>	15:8	0	RSSI Seek Threshold 0x00 = min RSSI (default) 0xFF = max RSSI SEEKTH presents the logarithmic RSSI threshold for the seek operation. The BK1080 will not validate channels with RSSI below the SEEKTH value. SEEKTH is one of multiple parameters that can be used to validate channels.
			BAND<1:0>	7:6	0	Band Select 00 = 87.5–108 MHz (US/Europe, Default) 01 = 76–108 MHz (Japan wide band) 10 = 76–90 MHz (Japan) 11 = 64-76MHz (except BK1080QB)
			SPACE<1:0>	5:4	0	Channel Spacing 00 = 200 kHz (USA, Australia) (default) 01 = 100 kHz (Europe, Japan) 10 = 50 kHz
			VOLUME<3:0>	3:0	0	Volume 0000 = mute (default) 0001 = –28 dB FS :: 1110 = –2 dB FS 1111 = 0 dB FS FS = Full Scale Volume scale is logarithmic
REG6	06h	R/W	System configuration 3. Default value: 0x0000			
			SMUTER<1:0>	15:14	0	Soft mute Attack/Recover Rate 00 = fastest (default) 01 = fast 10 = slow 11 = slowest
			SMUTEA<1:0>	13:12	0	Soft mute Attenuation 00 = 16 dB (default) 01 = 14 dB 10 = 12 dB 11 = 10 dB
			Reserved	11:8	0	Reserved, always write to 0

Register Name	Address	Dir	Name	Bits	Default (Hex)	Description
			SKSNR<3:0>	7:4	0	Seek SNR Threshold 0000 = disabled (default) 0001 = min (most stops) 1111 = max (fewest stops) Required channel SNR for a valid seek channel
			SKCNT<3:0>	3:0	0	Seek FM Impulse Detection Threshold 0000 = disabled (default) 0001 = max 1111 = min Allowable number of FM impulses for a valid seek channel
REG7	**07h**	**R/W**	**Test 1. Default value: 0x0000**			
			FREQD[11:0]	[15:4]	0	Frequency deviation. 148Hz on bit
			SNR[3:0]	[3:0]	0	SNR value
REG8	**08h**	**R/W**	**Test 2. Default value: 0x0000**			
			Reserved	15		Reserved, always write to 0
			Reserved	14:0	0	Reserved If written, these bits should be read first and then written with their pre-existing values. Do not write during power up
REG9	**09h**	**R/W**	**Boot configuration. Default value: 0x0000**			
			Reserved	15:0	0	Reserved If written, these bits should be read first and then written with their pre-existing values. Do not write during power up
REG10	**0Ah**	**R**	**RSSI Status. Default value: 0x0000**			
			Reserved	15	0	Reserved, always write to 0
			STC	14	0	Seek/Tune Complete 0 = Not complete (default) 1 = Complete The seek/tune complete flag is set when the seek or tune operation completes. Setting the SEEK 02h[8] or TUNE 03h[15] bit low will clear STC
			SF/BL	13	0	Seek Fail/Band Limit 0 = Seek successful 1 = Seek failure/Band limit reached The SF/BL flag is set high when SKMODE 02h[10] = 0 and the seek operation fails to find a channel qualified as valid according to the seek parameters The SF/BL flag is set high when SKMODE 02h[10] = 1 and the upper or lower band limit has been reached The SEEK 02h[8] bit must be set low to clear SF/BL
			AFCRL	12	0	AFC Rail 0 = AFC not railed 1 = AFC railed, indicating an invalid channel. Audio output is soft muted when set AFCRL is updated after a tune or seek operation completes and indicates a valid or invalid channel. During normal operation, AFCRL is updated to reflect changing RF environments
			Reserved	11:10	0	Reserved, always write to 0

Register Name	Address	Dir	Name	Bits	Default (Hex)	Description
			STEN	9	0	Stereo Decoder Indicator 0 = Mono 1 = Stereo Indicate the demodulated signal status, mono or stereo. This status is also available on GPIO3 by setting GPIO3 [5:4] = 01
			ST	8	0	Stereo Indicator 0 = Mono 1 = Stereo Indicate the received signal status, mono or stereo
			RSSI<7:0>	7:0	0	RSSI (Received Signal Strength Indicator). RSSI is measured units of dBμV in 1 dB increments with a maximum of approximately 75 dBμV 0x00 = Minimum signal strength 0xFF = Maximum signal strength RSSI will not report RF levels above 75 dBμV
REG11	**0Bh**	**R**	**Read channel. Default value: 0x0000**			
			Reserved	15:14	0	Reserved, always write to 0
			IMPC[3:0]	13:10	0	Impulse counter
			READCHAN<9:0>	9:0	0	Read Channel. If BAND 05h[7:6] = 00, then Freq (MHz) = Spacing (kHz) x Channel + 87.5 MHz If BAND 05h[7:6] = 01, BAND 05h[7:6] = 10, then Freq (MHz) = Spacing (kHz) x Channel + 76 MHz READCHAN [9:0] provides the current tuned channel and is updated during a seek operation and after a seek or tune operation completes. Spacing and channel are set with the bits SPACE 05h [5:4] and CHAN 03h[9:0]
REG12	**0Ch**	**R**	**Reserved**			
			Reserved	15:0	0	Reserved, always write to 0
REG13	**0Dh**	**R**	**Reserved**			
			Reserved	15:0	0	Reserved, always write to 0
REG14	**0Eh**	**R**	**Reserved**			
			Reserved	15:0	0	Reserved, always write to 0
REG15	**0Fh**	**R**	**Reserved**			
			Reserved	15:0	0	Reserved, always write to 0
REG16-33	**10h-1Fh**	**W**	**Internal test register, not visible for user. Initial value and procedure will be provided separately by BEKEN.**			

9 Typical Application Schematic

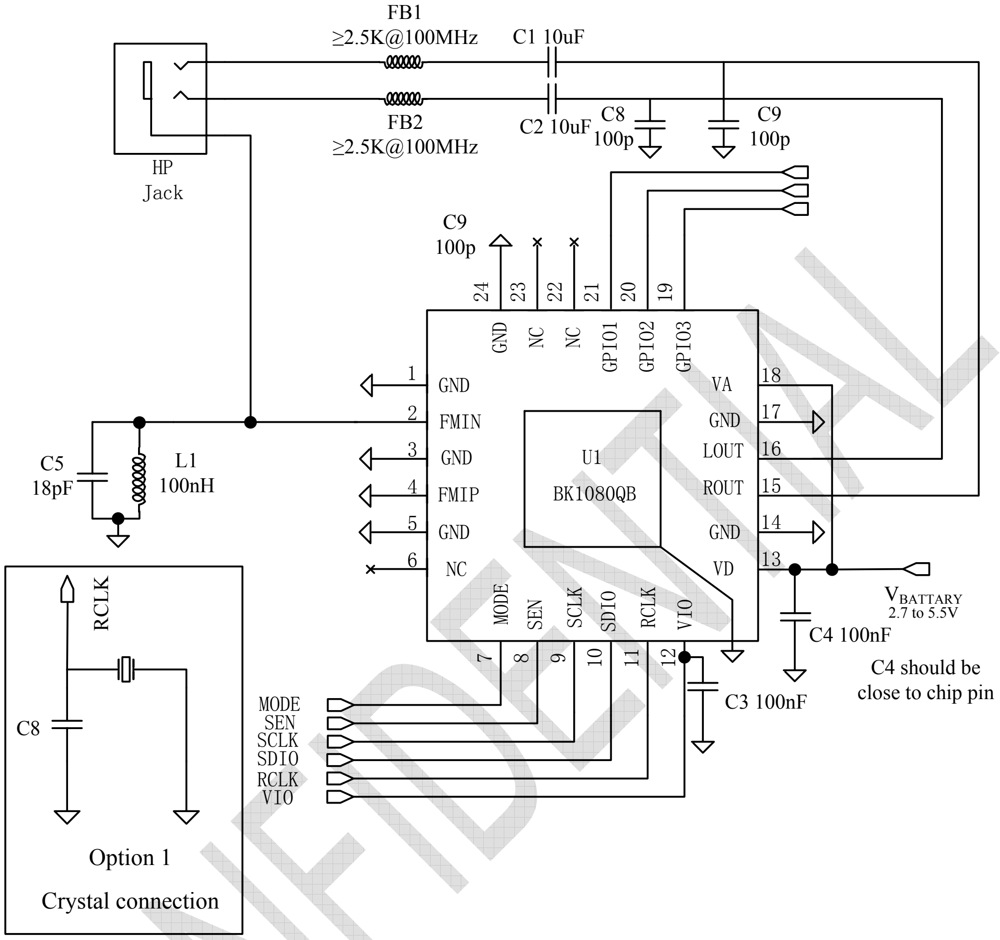


Figure 13. BK1080QB with Single-ended Input Application

Notes:

1. J1: Common 32Ω resistance headphone.
2. U1: BK1080QB chip.
3. FM choke (L1 and C5) for LNA input match with the headphone.
4. Pin NC (22, 23) should be leaved floating.
5. Place C3 and C4 close to chip pin.
6. When BK1080QB use crystal to generate the reference clock, please refer to the option1.
7. All grounds connect directly to GND plane on PCB.
8. Keep the FMIP trace as short as possible.
9. Keep the wire from FMIN to headphone as short as possible and must put it on the surface of the PCB.

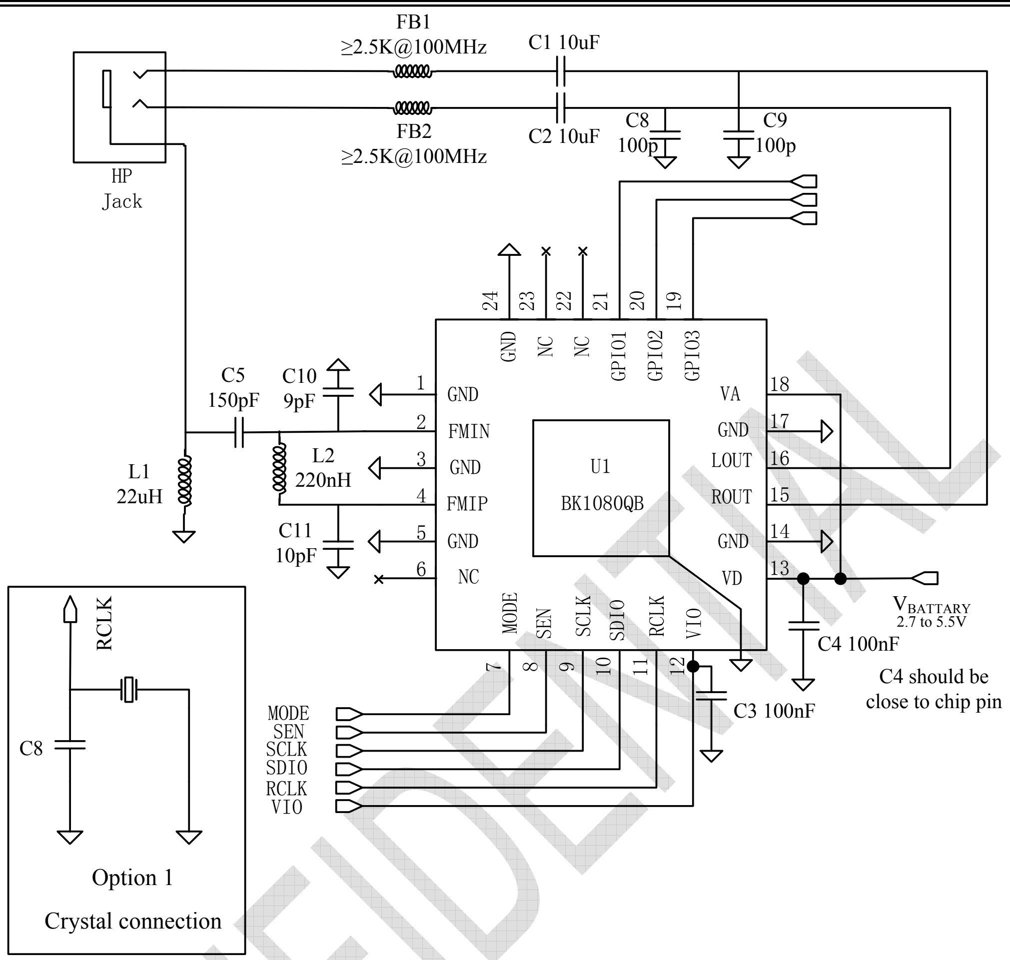


Figure 14. BK1080QB with Differential Input Application

Notes:

1. J1: Common 32Ω resistance headphone.
2. U1:BK1080QB chip.
3. Pin NC (22, 23) should be leaved floating.
4. Place C3 and C4 close to chip pin.
5. When use crystal to generate the reference clock, please refer to the option 1(Crystal connection).
6. All grounds connect directly to GND plane on PCB.
7. Keep the FMIP trace as short as possible.
8. Keep the wire from FMIN to headphone as short as possible and must put it on the surface of the PCB.
9. Application with differential input improved system sensitivity 3dB.

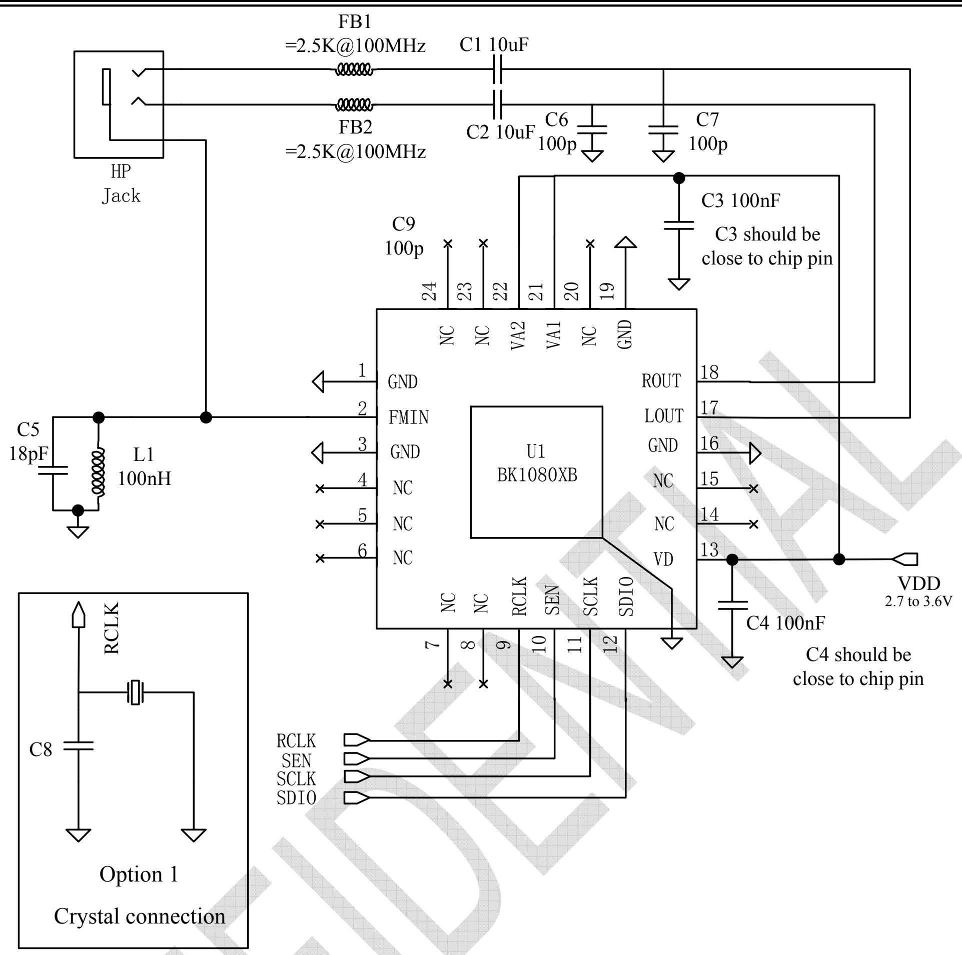


Figure 15. BK1080XB with Single-ended Input Application

Notes:

1. J1: Common 32Ω resistance headphone.
2. U1: BK1080XB chip.
3. FM choke (L1 and C5) for LNA input match with the headphone.
4. All NC pin should be leaved floating.
5. BK1080XB can't use crystal to generate the reference clock.
6. Place C3 and C4 close to chip pins.
7. All grounds connect directly to GND plane on PCB.
8. Keep the wire from FMIN to headphone as short as possible and must put it on the surface of the PCB.

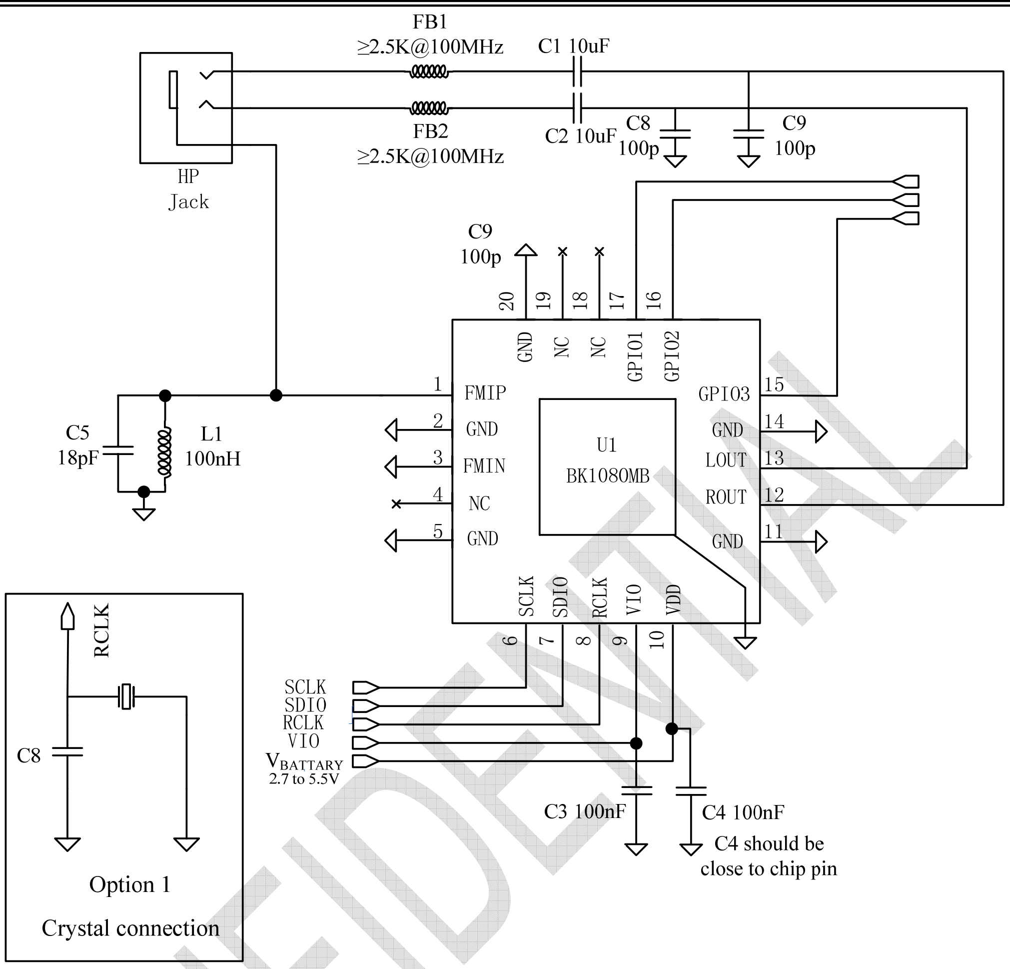


Figure 16. BK1080MB with Single-ended Input Application

Notes:

1. J1: Common 32Ω resistance headphone.
2. U1: BK1080MB chip.
3. FM choke (L1 and C5) for LNA input match with the headphone.
4. All NC pin should be leaved floating.
5. Place C3 and C4 close to chip pin.
6. BK1080MB can't use crystal to generate the reference clock.
7. All grounds connect directly to GND plane on PCB.
8. Keep the FMIN trace as short as possible.
9. Keep the wire from FMIP to headphone as short as possible and must put it on the surface of the PCB.

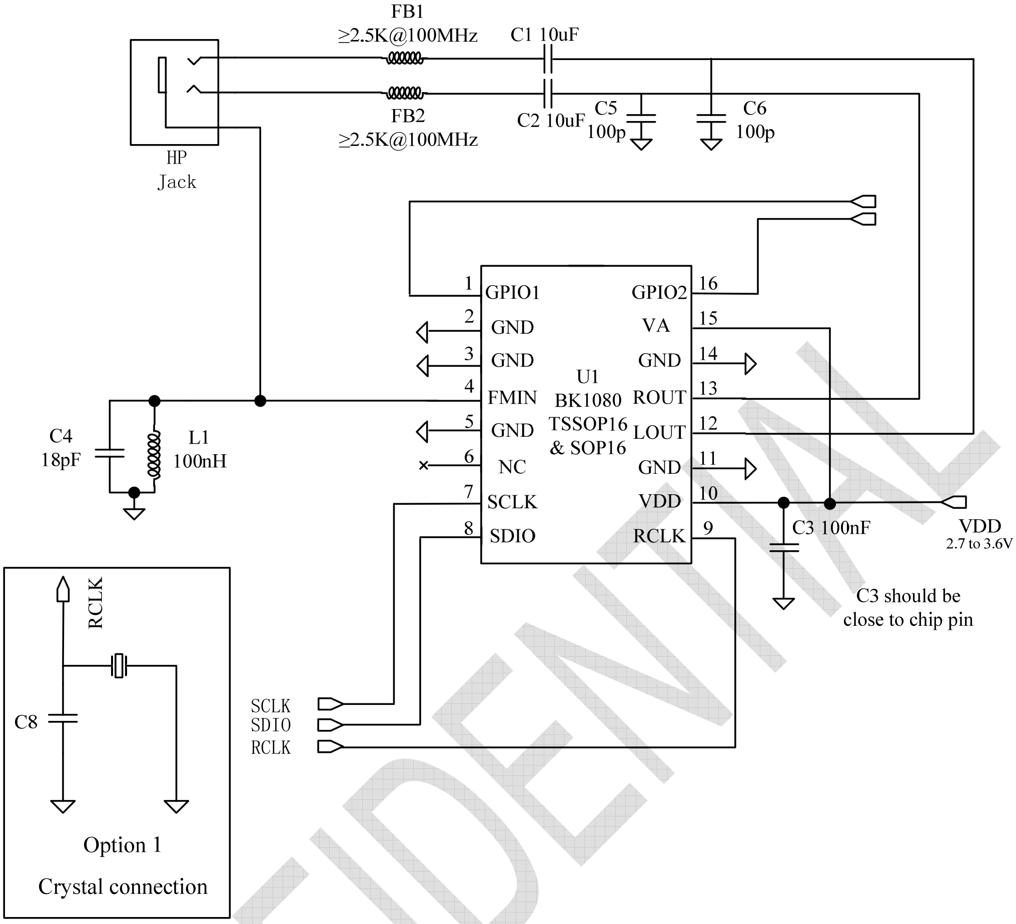


Figure 17. BK1080TB and BK1080SB with Single-ended Input Application

Notes:

1. J1: Common 32Ω resistance headphone.
2. U1: BK1080TB or BK1080SB chip.
3. FM choke (L1 and C4) for LNA input match with the headphone.
4. All NC pin should be leaved floating.
5. BK1080TB and BK1080SB can't use crystal to generate the reference clock.
6. Place C3 close to chip pin.
7. All grounds connect directly to GND plane on PCB.
8. Keep the wire from FMIN to headphone as short as possible and must put it on the surface of the PCB.

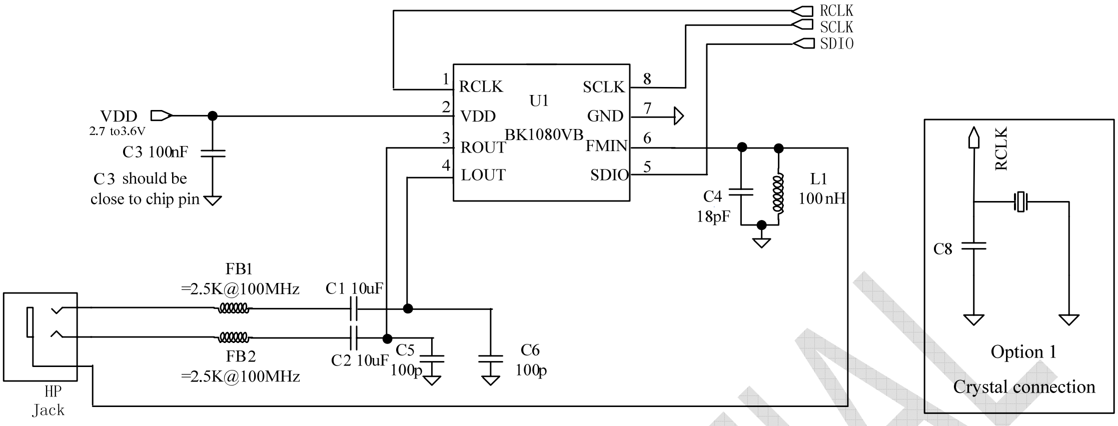


Figure 18. BK1080VB with Single-ended Input Application

Notes:

1. J1: Common 32Ω resistance headphone.
2. U1: BK1080VB chip.
3. FM choke (L1 and C4) for LNA input match with the headphone.
4. BK1080VB can't use crystal to generate the reference clock.
5. Place C3 close to chip pin.
6. Keep the wire from FMIN to headphone as short as possible and must put it on the surface of the PCB.

10 Package information

We have chosen QFN 4x4 24pin, QFN 3x3 20pin, TSSOP 16pin and SOP 16pin, SOP8 pin packages. Detail information of the package follows:

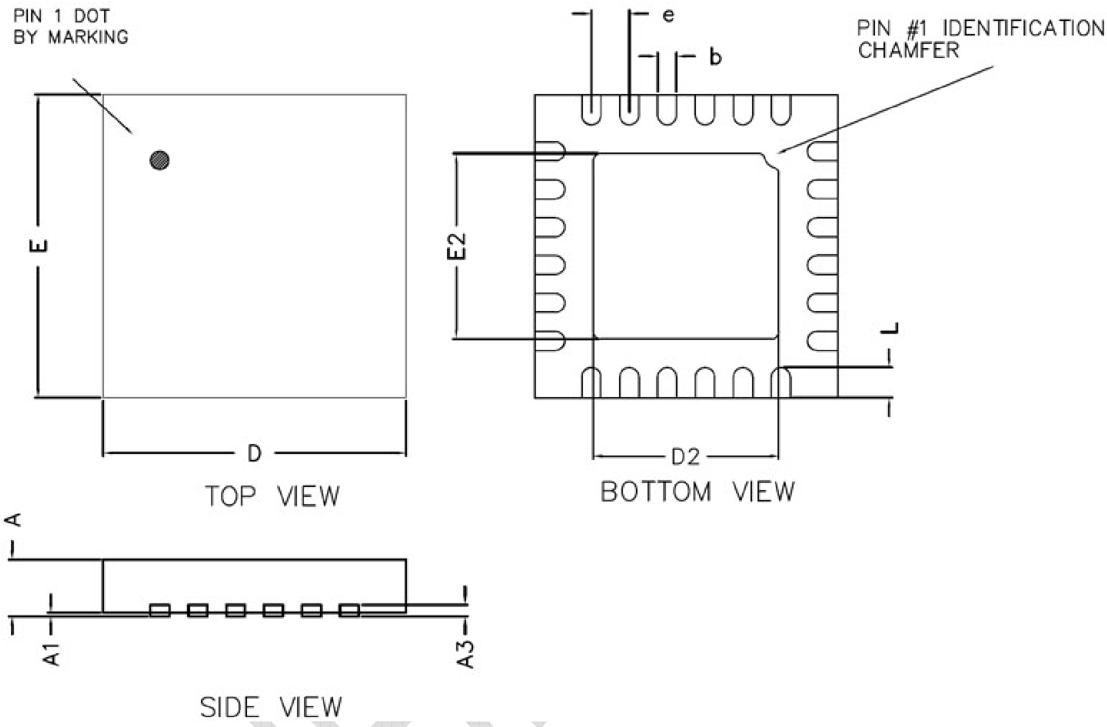


Figure 19 QFN 4x4 24 Pin Package diagram

Table 12 QFN 4x4 24 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0.00	0.02	0.05	mm
A3		0.20 REF		mm
D	3.95	4.00	4.05	mm
E	3.95	4.00	4.05	mm
b	0.20	0.25	0.30	mm
L	0.35	0.40	0.45	mm
D2	2.30	2.45	2.55	mm
E2	2.30	2.45	2.55	mm
e		0.50 REF		mm

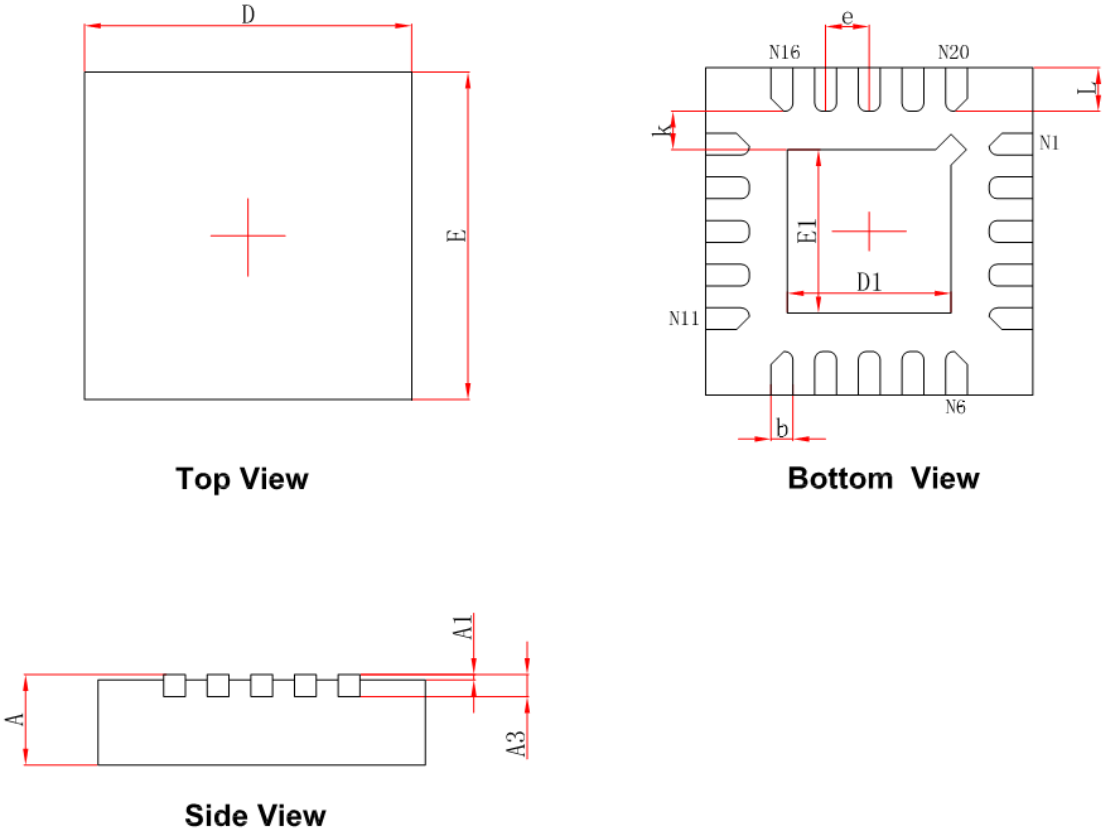


Figure 20 QFN 3x3 20 Pin Package diagram

Table 13 QFN 3x3 20 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	0.700	0.750	0.800	mm
A1	0.000	0.025	0.050	mm
A3		0.203 REF		mm
D	2.924	3.000	3.076	mm
E	2.924	3.000	3.076	mm
b	0.150	0.200	0.250	mm
L	0.324	0.400	0.476	mm
D1	1.400	1.500	1.600	mm
E1	1.400	1.500	1.600	mm
e		0.40 REF		mm

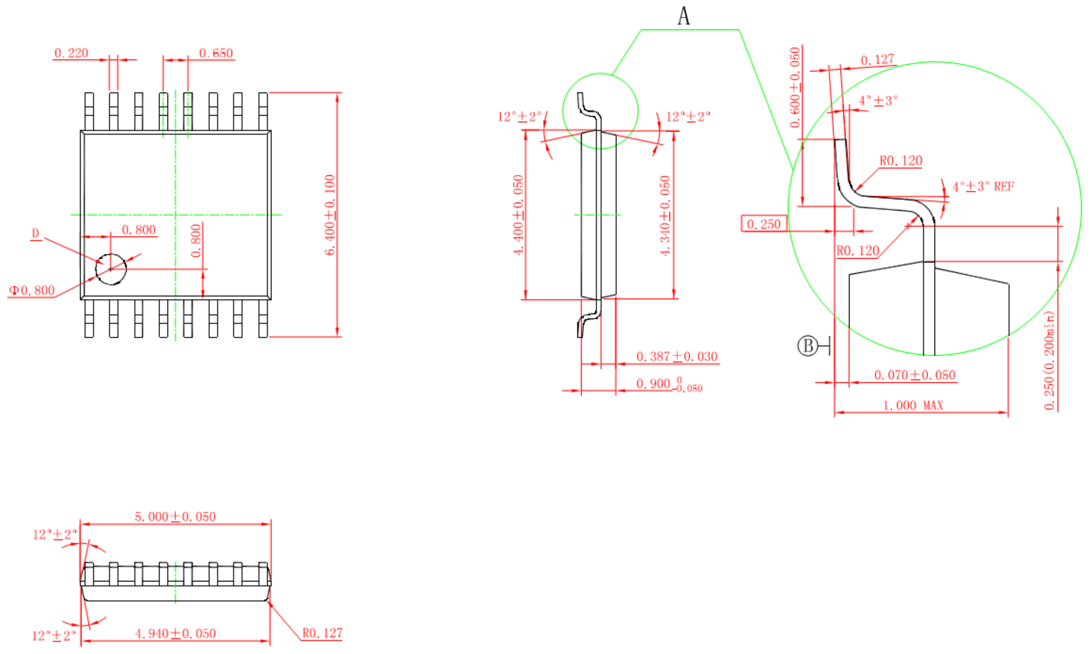


Figure 21 TSSOP 16 Pin Package diagram

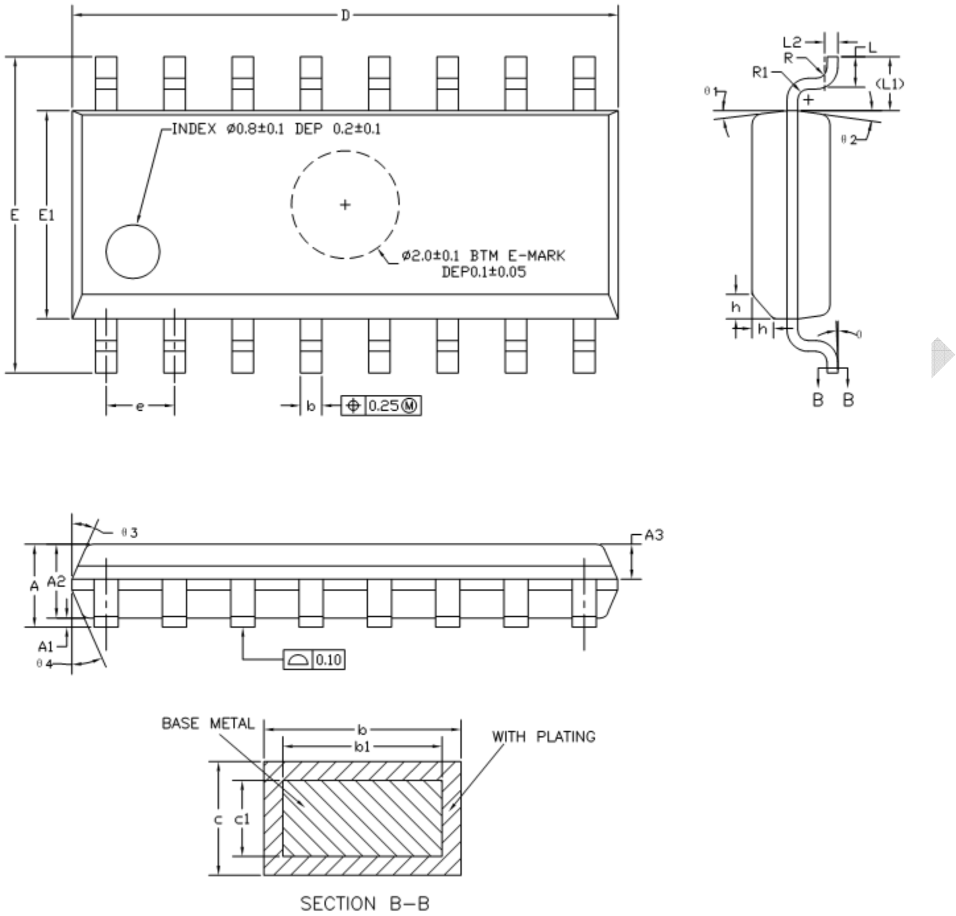
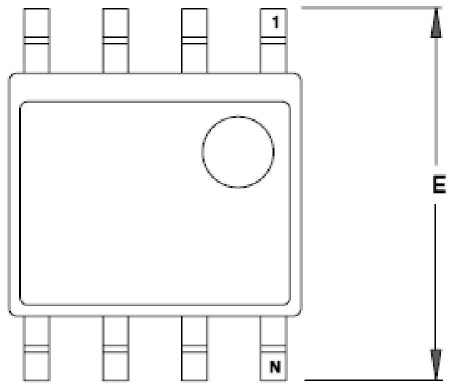


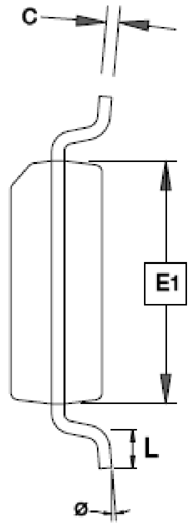
Figure 22 SOP 16 Pin Package diagram

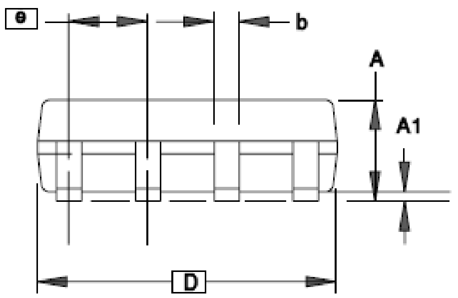
Table 14 SOP 16 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	1.35	1.60	1.75	mm
A1	0.10	0.15	0.25	mm
A2	1.25	1.45	1.65	mm
A3	0.55	0.65	0.75	mm
b	0.36	-	0.51	mm
b1	0.35	0.40	0.45	mm
c	0.17	-	0.25	mm
c1	0.17	0.20	0.23	mm
D	9.80	9.90	10.00	mm
E	5.80	6.00	6.20	mm
E1	3.80	3.90	4.00	mm

e	1.27 BSC			mm
L	0.45	0.60	0.80	mm
L1	1.04 REF			mm
L2	0.25 BSC			mm
R	0.07	-	-	mm
R1	0.07	-	-	mm
h	0.30	0.40	0.50	mm
θ	0	-	8	°
θ1	6	8	10	°
θ2	6	8	10	°
θ3	5	7	9	°
θ4	5	7	9	°







COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Figure 23 SOP 8 Pin Package diagram

Soldering Layer Content

Content	width	unit
Ni	0.5-2.0	um
Pd	0.02-0.15	um
Au	0.003-0.015	um

Storage Caution

1. Calculated shelf life in vacuum sealed bag 12 months at<40℃ and 90% relative humidity(RH).
2. Peak package body temperature 260℃.
3. After vacuum sealed bag is opened ,devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within 168 hours of factory conditions<40℃/60%.
   b) Stored at 10% RH.

11 Solder Reflow Profile

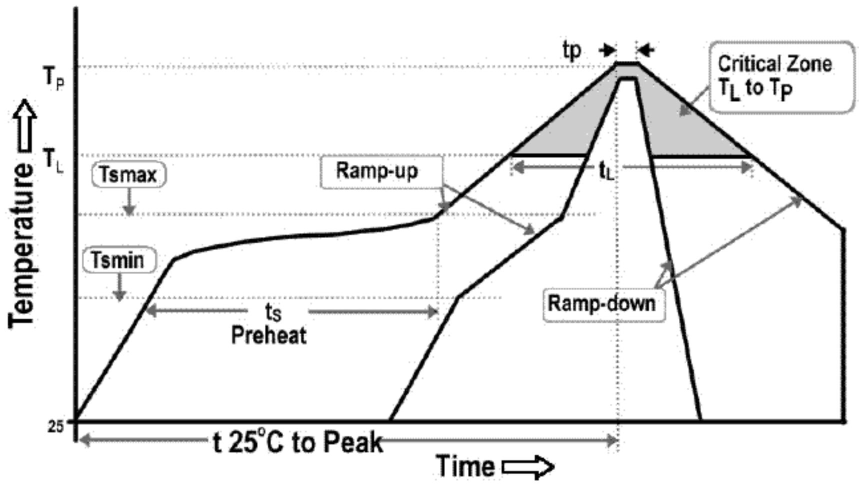


Figure 24 Classification Reflow Profile

Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3°C/second max.
Pre_heat	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (TL)	217°C
	Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual PeakTemperature (tp)		20-40 seconds
Ramp-Down Rate 6		6°C/second max.
Time 25°C to Peak Temperature 8		8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD Techniques should be used when handling these devices.

12 Order information

Table 15 BK1080 order information

Part number	Package	Packing	MOQ (ea)
BK1080QB	QFN24	Tape Reel	3K
BK1080XB	QFN24	Tape Reel	3K
BK1080MB	QFN20	Tape Reel	3K
BK1080TB	TSSOP16	Tape Reel	3K
BK1080SB	SOP16	Tape Reel	3K
BK1080VB	SOP8	Tape Reel	3K

Remark:
MOQ: Minimum Order Quantity